library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_arith.all;

entity converter is

port(Excess: in std\_logic\_vector(3 downto 0);

BCD: out std\_logic\_vector(3 downto 0));

end converter;

architecture CONV of converter is

begin

process(Excess)

begin

case Excess is

when "0011" => BCD<="0000";

when "0100" => BCD<="0001";

when "0101" => BCD<="0010";

when "0110" => BCD<="0011";

when "0111" => BCD<="0100";

when "1000" => BCD<="0101";

when "1001" => BCD<="0110";

when "1010" => BCD<="0111";

when "1011" => BCD<="1000";

when "1100" => BCD<="1001";

when "1101" => BCD<="1010";

when "1110" => BCD<="1011";

when "1111" => BCD<="1100";

when others => BCD<="0000";

end case;

end process;

end CONV;